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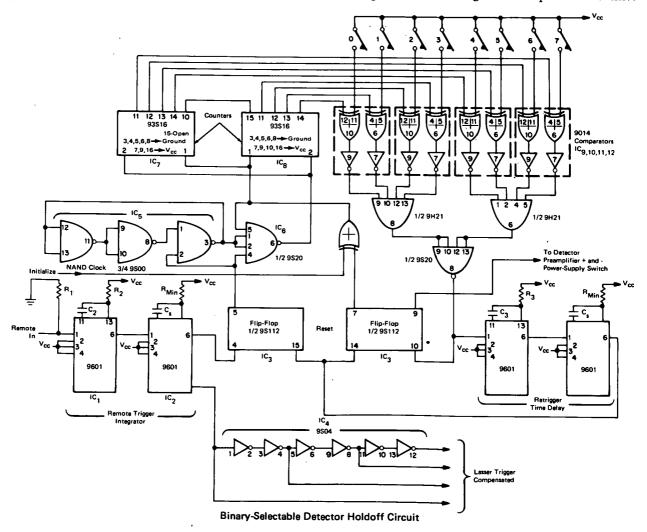


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Binary-Selectable Detector Holdoff Circuit

The problem:

The application of laser/radar systems to the study of the lower atmosphere has been hampered severely by a very large dynamic range of the backscatter signal return. Basically, there have been two approaches to this problem. In the first approach, multiple detectors are utilized, with each detector having a different linearamplifier, signal-gain factor. In the second approach, fixed-gain logarithmic amplifiers are utilized to compress the dynamic range of the returned signal. Although each of these approaches is applicable, neither addresses itself to the problem concerning the overexposure of sensitive



(continued overleaf)

detectors to the sudden, extremely-intense backscattered radiation that results from short-range atmospheric dust layers, or low-level clouds, entering the laser/radar field of view.

The solution:

A very high-speed switching circuit has been designed to protect these detectors.

How it's done:

The function of the circuit is to provide computer-controlled switching of the photodiode detector, pre-amplifier power-supply voltages, typically less than ±20 volts, in approximately 10 nanoseconds. To reduce system noise, the power-supply voltages are switched, rather than the photodiode-detector input, to the preamplifier. The circuit is shown in the illustration.

When a high-low-high (HLH) or a low-high-low (LHL) remote pulse is applied, the Q output of the one-shot multivibrator integrated circuit (IC₁) is triggered. The combination of C₂ and R₂ establishes the longest time delay of the entire circuit to prevent retriggering. Since the Q output is an HLH pulse, IC₂ triggers immediately on the lagging pulse edge. C_s is simply a stray capacitance, and R_{min} is chosen to provide an output pulse width greater than 100 nanoseconds. The Q output (LHL) pulse provides the true laser trigger, and the Q output (HLH) presets one flip-flop of the IC₃. The 100-nanosecond laser-trigger pulse is sent through hex inverter pairs (IC₄) to provide for a delay of the laser-trigger output pulse. The delay range available is from 54 to 360 nanoseconds.

When IC₃ is preset, NAND gate clock IC₅ is synchronized and clock pulses are passed through NAND gate IC₆. The clock pulses are counted by the dual converters, IC₇ and IC₈. The counter outputs are being compared constantly to the sense-line settings by the EXCLUSIVE OR gates, IC₉, 10, 11, 12. When a true comparison is achieved, NAND gate IC₆ produces an HLH pulse. This pulse presets the second flip-flop of IC₃ and turns on the preamplifier power-supply switch. In addition, the pulse stops the NAND gate clock output, resets the counters, and initiates the retrigger time delay of the one-shot multivibrator.

Note:

Requests for further information may be directed to:
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Patent status:

Inquiries concerning rights for the commercial use of this invention should be addressed to:

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